Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.046”**

**.051”**

**2 1 14 13 12**

**6 7 8**

**11**

**10**

**9**

**3**

**4**

**5**

**+**

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **Vcc**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .046” X .051” DATE: 1/24/23**

**MFG: MOTOROLA THICKNESS .015” P/N: 5408**

**DG 10.1.2**

#### Rev B, 7/19/02